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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,234	12/06/2001	Masatoshi Anma	50090-458	4496

7590 06/05/2002

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,234	ANMA, MASATOSHI	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the said load circuit and said short circuit or spare circuit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 6 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. The said "short circuit or spare circuit", "predetermined void" and said "by way of predetermined void" are not understood. Clarification is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1-6, as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Sur, Jr. et al. US Patent No. 5,764,563.

Sur, Jr. et al disclose in fig. 4 a semiconductor device having a short circuit or spare circuit for preventing application of a high voltage to a load circuit, comprising a substrate 430; a first interconnection 242 formed on said substrate and connected to the short circuit or spare circuit; a first dielectric film 334 for covering said first interconnection; an opening section for extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film; a plug 316 formed in said opening section and electrically connected to said first interconnection; a second interconnection 240 having a barrier metal layer and an aluminum interconnection formed on the barrier metal layer (as in claims 2, 4 and 5) formed on said plug by way of a determined void or second interconnection 240 formed on said first dielectric film in the vicinity of said plug (as in claim 6) and connected to the load circuit 308; and a second dielectric film 346 or second dielectric film 346 having a predetermined void located at a position above said plug (as in claim 6) and covering said second interconnection.

As to the formation of the said void by various means recited in claims 1-5, "product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

7. Claims 1, 2, 4-6, as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Gordon et al. US Patent No 5,786,268.

Gordon et al disclose (see figs. 7, 9, 10, 12, col. 8, lines 1-8 and col. 12, lines 1-12) a semiconductor device having a short circuit or spare circuit for preventing application of a high voltage to a load circuit, comprising a substrate; a first interconnection 538 formed on said substrate and connected to the short circuit or spare circuit; a first dielectric film 540 for covering said first interconnection; an opening section for extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film; a plug 545 formed in said opening section and electrically connected to said first interconnection; a second interconnection 26, 27 having a barrier metal layer and an aluminum interconnection formed on the barrier metal layer (as in claims 2, 4 and 5) formed on said plug by way of a determined void or second interconnection 26, 27 formed on said first dielectric film in the vicinity of said plug (as in claim 6) and connected to the load circuit (unnumbered); and a second dielectric film 320 or second dielectric film having a

predetermined void located at a position above said plug (as in claim 6) and covering said second interconnection.

8. Claims 1 and 6, as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Sur, Jr. et al. US Patent No 6,143,642.

Sur, Jr. et al disclose in fig. 3 a semiconductor device having a short circuit or spare circuit for preventing application of a high voltage to a load circuit, comprising a substrate; a first interconnection 304' formed on said substrate and connected to the short circuit or spare circuit; a first dielectric film 310 for covering said first interconnection; an opening section for extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film; a plug 312 formed in said opening section and electrically connected to said first interconnection; a second interconnection 314' formed on said plug by way of a determined void or second interconnection 314' formed on said first dielectric film in the vicinity of said plug (as in claim 6) and connected to the load circuit (unnumbered); and a second dielectric film 317 or second dielectric film having a predetermined void 320 located at a position above said plug (as in claim 6) and covering said second interconnection.

9. Claim 15, as understood, is rejected under 35 U.S.C. 102(e) as being anticipated by Anma et al. US Patent No 6,319,812.

Anma et al disclose in fig. 1 a semiconductor device having a short circuit or spare circuit for preventing application of a high voltage to a load circuit, comprising a substrate; a first dielectric film 16 formed on said substrate and having an opening

section; a pad 18 formed in the opening section and having conductivity; a first interconnection 20 formed on said first dielectric film such that a portion of the bottom of said first interconnection comes into contact with an upper surface of said pad; a second interconnection 1 formed on said first dielectric film such that a portion of the bottom of said second interconnection does not come into contact with the upper surface of said pad, said second interconnection being connected to the load circuit, said pad being disposed between said first and said second interconnections; and a second dielectric film 2 having a predetermined void located at a position on said pad, said second dielectric film covering said firs and second interconnection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
June 2, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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